IC-R3 CIRCUIT DESCRIPTION

1 RECEIVER CIRCUITS

1-1 RF SWITCHING CIRCUIT (RF UNIT)

(1) Below 1150 MHz

The RF signals from the antenna connector pass through the band switching diode (D2) and an attenuator (D12, D13). The signals are then applied to the RF circuit which suppress out-of-band signals via the band switching circuit (D911).

(2) Above 1150 MHz

The RF signals from the antenna connector pass through the limitter (D1), the band switching diode (D909) and the high-pass filter (C932–C936, C963, C964, L911, L912, L914). The filtered signals are applied to the AF amplifier (IC14, pin 1), and are then applied to the convertor circuit (IC13, pin 1). The convertor circuit mixes with “CONLO” signal from [CONV VCO] circuit to down convert above 1150 MHz RF signal to below 1150 MHz RF signal. The converted signals output IC13 (pin 6), and are then applied to the RF circuit which suppress out-of-band signals.

1-2 RF CIRCUIT (RF AND RF-B UNITS)

The RF circuit amplifies the received signals within the range of frequency coverage and filters out-of-band signals.

(1) 0.495 MHz–29.995 MHz

RF signals (0.495MHz–29.995MHz) from the RF switching circuit pass through a low-pass filter (C321–C325, L81, L82). The filtered signals are amplified at an RF amplifier (Q3) passing through each low-pass, bandpass, high-pass filter depending on the receiving frequency. The amplified signals are then applied to the 1st mixer circuit (IC1) via the band switching diode (D10).

The signals below 1.9 MHz pass through a low-pass filter (C344–C347, L89, L90) via the band switching diode (D4), and are then applied to the RF amplifier circuit (Q3) via the band switching diode (D7).

The 1.9 MHz–14.995 MHz signals pass through the band switching diode (D5) and bandpass filter (C332–C341, L85–L88), and are then applied to the RF amplifier circuit (Q3) via the band switching diode (D8).

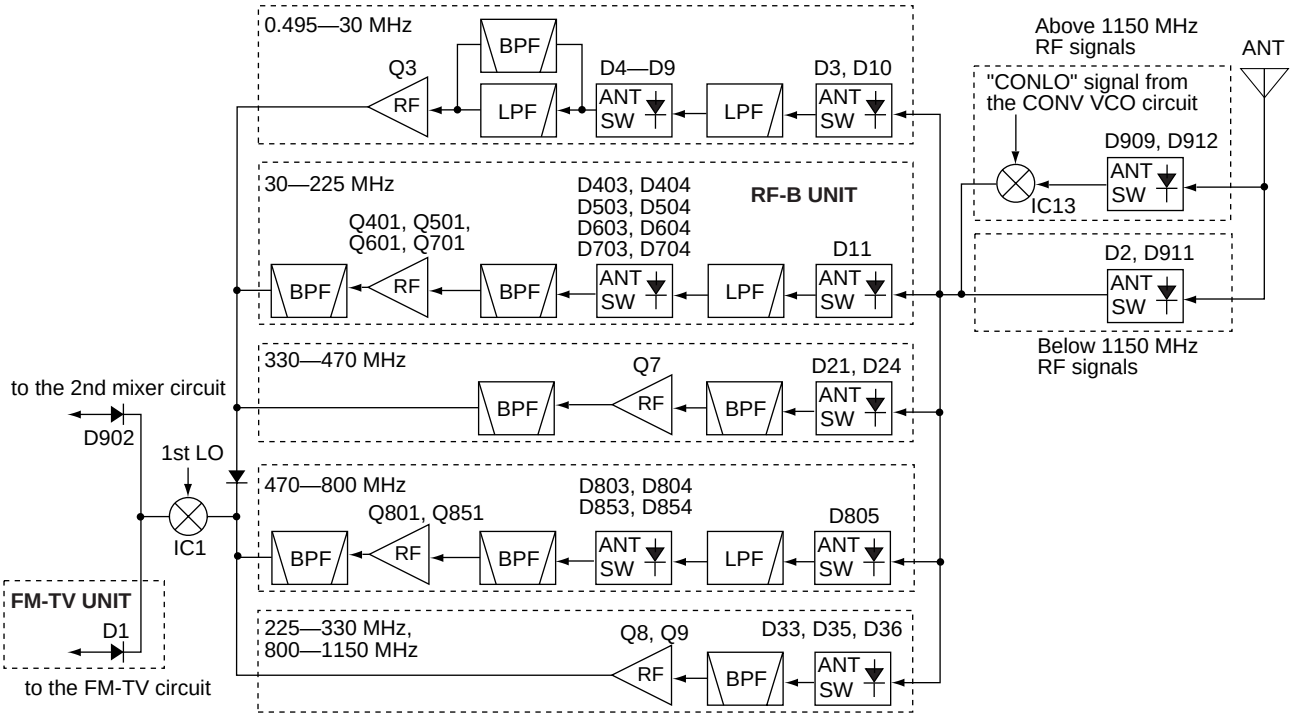
The 15 MHz–29.995 MHz signals pass through the band switching diode (D6) and high-pass filter (C326–C330, L83, L84) and are then applied to the RF amplifier circuit (Q3) via the band switching diode (D9).

(2) 30 MHz–224.995 MHz (RF-B UNIT)

RF signals (30 MHz–64.995 MHz, 65 MHz–107.995.995 MHz, 108 MHz–173.995 MHz, 174 MHz–224.995 MHz) from the RF switching diode (RF unit;D11) are passed through low-pass filter (RF unit; C12–C17, L57–L59). The filtered signals pass through the each bandpass filters and the RF amplifier depending on the receiving frequency. The filtered signals are then applied to the 1st mixer circuit (RF unit;IC1).

The 30 MHz–64.995 MHz signals pass through the band switching diode (D403) and bandpass filter (D401), and are then amplified at the RF amplifier (Q401). The amplified signal passes the bandpass filters (D402) and the band switching diode (D404).

• RF CIRCUIT



The 65 MHz–107.995 MHz signals pass through the band switching diode (D503) and bandpass filter (D501), and are then amplified at the RF amplifier (Q501). The amplified signal passes the bandpass filters (D502) and the band switching diode (D504).
The 108 MHz–173.995 MHz signals pass through the band switching diode (D603) and bandpass filter (D601), and are then amplified at the RF amplifier (Q601). The amplified signal passes the bandpass filters (D602) and the band switching diode (D604).

The 174 MHz–224.995 MHz signals pass through the band switching diode (D703) and bandpass filter (D701), and are then amplified at the RF amplifier (Q701). The amplified signal passes the bandpass filters (D702) and the band switching diode (D704).

(3) 330 MHz–469.995 MHz
RF signals (330MHz–469.995MHz) from the RF switching circuit pass through the band switching circuit (D21) and a bandpass filter (C19–C27, L2–L5, L39). The filtered signals are amplified at an RF amplifier (Q7), and then passing through the bandpass filter (D22, D23). The filtered signals are then applied to the 1st mixer circuit (IC1) via the band switching diode (D24).

(4) 470 MHz–799.995 MHz
RF signals (470MHz–799.995MHz) from the RF switching circuit pass through the band switching circuit (D805) and a low-pass filter (C321–C325, L81, L82). The filtered signals are passing through each bandpass filters and the RF amplifier depending on the receiving frequency. The amplified signals are then applied to the 1st mixer circuit (IC1) via the band switching diode (D804 or D854).

The 470 MHz–599.995 MHz signals pass through the band switching diode (D803) and bandpass filter (D801), and are then amplified at the RF amplifier (Q801). The amplified signal passes the bandpass filters (D802) and the band switching diode (D804).

The 600 MHz–799.995 MHz signals pass through the band switching diode (D853) and bandpass filter (D851), and are then amplified at the RF amplifier (Q851). The amplified signal passes the bandpass filters (D852) and the band switching diode (D854).

(5) 225 MHz–329.995 MHz AND 800 MHz–1149.995 MHz
RF signals (225MHz–329.995MHz and 800MHz–1149.995 MHz) from the RF switching circuit pass through the band switching circuit (D33). Thesignals are passing through each bandpass filters and the RF amplifier depending on the receiving frequency. The amplified signals are then applied to the 1st mixer circuit (IC1) via the band switching diode (D35 or D36).

The 225 MHz–329.995 MHz signals pass through the bandpass filter (C40–C43, C395, C396,L58, L59), and are then amplified at the RF amplifier (Q9). The amplified signal passes the band switching diode (D35).

The 800 MHz–1149.995 MHz signals pass through the bandpass filter (C46–C49, C51–C54, L11–L14), and are then amplified at the RF amplifier (Q8). The amplified signal passes the band switching diode (D36).

1-3 1ST MIXER CIRCUIT (RF UNIT)

The 1st mixer circuit converts the received RF signals to a fixed frequency of the 1st IF signal with a PLL output frequency. By changing the PLL frequency, only the desired frequency will pass through the bandpass filters at the next stage of the 1st mixer.

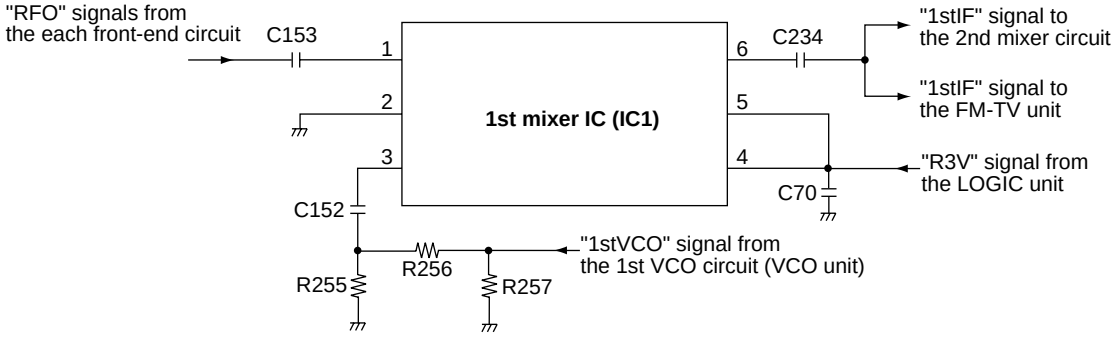
The each filtered or amplified RF signals are mixed with 1st LO signals at the 1st mixer circuit (IC1) to produce each 1st IF signals depending on the receiving frequency. The 1st IF signal is output from pin 6, and passed through the bandpass filter (FI904) to suppress unwanted harmonic components. The filtered 1st IF signal is applied to the 2nd mixer circuit.

	FM, AM, WFM	C3F (TV)
1ST IF	240.1MHz	241.85*[1], 238.35*[2] MHz

*[1]30–799.995 MHz and 1321–2099.995 MHz range
*[2]800–1320.995 MHz and 2100–2450.095 MHz range

The 1st LO signals are generated at the 1st VCO (VCO unit; Q22, Q23, D62) and are applied to the 1st mixer (IC1, pin 3) directly or passing through the doubler circuit (Q26) after being amplified at the buffer amplifiers (VCO unit; IC4).

• 1ST MIXER CIRCUIT (RF UNIT)



1-4 1ST IF AND 2ND MIXER CIRCUITS (RF UNIT)

The 2nd mixer circuit converts the 1st IF signal to a 2nd IF signal.

The filtered each 1st IF signal from the bandpass filter are mixed with the 2nd LO signal at the 2nd mixer circuit (IC10, pin 1) to produce each 2nd IF signal depending on the receiving frequency.

In AM and FM mode, the 2nd IF signals (26.5 MHz) pass through the band switching diode (D71) and the bandpass filter (FI3). The filtered signals are then amplified at the 2nd IF amplifier (Q41), and are applied to the demodulator circuit.

In WFM mode, the 2nd IF signal (13.25 MHz) passes through the band switching diode (D72) and the bandpass filter (FI4). The filtered signal is then amplified at the 2nd IF amplifier (Q41), and is applied to the demodulator circuit.
In TV mode, the 2nd IF signal (58.75 MHz) passes through the band switching diode (D901), is then applied to the 2nd IF amplifier (Q901). The amplified signal passes through the bandpass filter (FI901), and is applied to the demodulator circuit.

1-5 DEMODULATOR CIRCUITS (RF UNIT)

The demodulator circuit converts the 2nd IF signal into AF signals or video signals.

(1) AM, FM AND WFM MODE

The each 2nd IF signals from the 2nd IF amplifier (Q41) are applied to the 3rd mixer section of the FM IF IC (IC2, pin 16) and are then mixed with the 3rd LO signal for conversion into a 450 kHz 3rd IF signal.

IC2 contains the 3rd mixer, limiter amplifier, quadrature detector and S-meter detector, etc. A frequency from the PLL reference oscillator (VCO unit; IC3) is used for the 3rd LO signal (12.80 MHz).

• AM MODE

The 3rd IF signal is output from FM IF IC (IC2, pin 3) and passes through the ceramic bandpass filter (FI2). The filtered IF signal is applied to the AM detector circuit (Q44, Q45) to converted into AF signals, and the signals are applied to the AF circuit (LOGIC unit).

• FM MODE

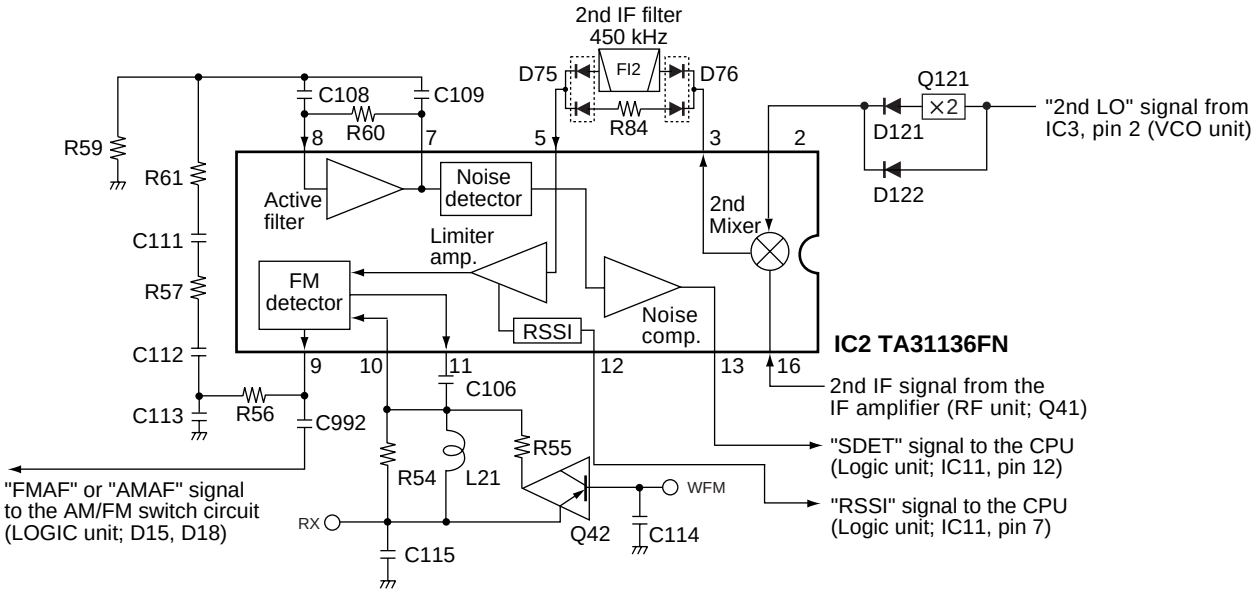
The 3rd IF signal is output from FM IF IC (IC2, pin 3) and passes through the ceramic bandpass filter (FI2). The filtered signal is fed back and amplified at the limiter amplifier section (pin 5), then demodulated AF signals at the quadrature detector section (pins 10, 11) and detector coil (L21). The demodulated AF signals are output from pin 9 and are applied to the AF circuit (LOGIC unit).

• WFM MODE

The 3rd IF signal from the 3rd mixer bypasses the ceramic filter (FI2) and fed back to the limiter amplifier section (pin 5). The amplified signal is demodulated at the quadrature detector section (pins 10, 11) and detector coil (L21). The AF signals are output from pin 9 and are applied to the AF circuit (LOGIC unit).

By connecting R55 to R54 in parallel, the output characteristics of pin 12, “RSSI”, change gradually. Therefore, the FM IF IC can detect WFM components.

• 2ND IF AND DEMODULATOR CIRCUITS (RF UNIT)



(2) TV MODE

The IF amplifed signals are applied to the bandpass filter (FI901). The filtered signals are applied to the TV IF IC (IC901) as the audio IF signal and the video IF signal, separately.
IC901 is the video/audio detector IC of the PLL sprit type, which contains the video IF amplifier, PLL video detector, voice IF detector, IF and RF AGC, etc.

The audio IF signal from FI901 (pin 3) is applied to the TV IF IC (IC901, pin 9) as the “SIF” signal, and is amplified and PLL detected in the IC. The detected signal is output from pin 15, and is fed back to the pin 13 via the FI902. The filtered signal is applied to the limitter amplifier section and the FM detector section in the TV IF IC.
The demodulated AF signals are output from pin 12 and are applied to the AF circuit (LOGIC unit).

The video IF signal from FI901 (pin 4, 5) is applied to the TV IF IC (IC901, pin 4, 5) as “VIF” signal, and is then amplified at the video IF amplifier in the TV IF IC. The amplified signal is compared to the VCO frequency (L902, C906), and is then applied to the PLL detector section in the TV IF IC. The detected signal is output from pin 22 as the video signal, and then passed through the bandpass filter (FI905). The filtered signal is amplified at Q854, and applied to the buffer amplifier (Q855). The amplified signal is applied to the TFT LCD circuit (LOGIC unit).

1-6 AF AMPLIFIER CIRCUIT (LOGIC UNIT)

The AF amplifier circuit amplifies the demodulated AF signals to drive a speaker.

While in FM and TV mode, AF signals (“FMAF” signal) from the demodulator circuit (RF unit) are passed through the de-emphasis circuit (R118, C66, C68) with frequency characteristics of –6 dB/octave, and are then applied to the pre-amplifier (Q31) via the band pass filter (Q30).

While in AM mode, AF signals (“AMAF” signal) are pass through the band-pass filter (Q30) and are then applied to the pre-amplifier (Q31).

While in WFM mode, AF signals (“WFM” signal) are applied to the pre-amplifier (Q31) directly.

The pre-amplified AF signals pass through the AF mute circuit (Q37) and are then applied to the electronic volume control circuit (IC14, pin 6). The level controlled AF signals are output from pin 7 and applied to the AF power amplifier (IC15, pin 1) via the buffer amplifier (Q36). The power amplified AF signals are applied to the internal speaker via the [EXT SP] jack.
The electronic volume control circuit controls AF gain, therefore, the AF output level is according to the [VOL] setting and also the squelch conditions. The AF mute circuit and the electronic volume control circuit are controlled by CPU (IC11) via each “AMUTE” and “VRC” signal.

When connecting [A/V OUT] jack(RF unit; J3) on TV mode, AF signals from demodulator circuit (RF unit; IC901, pin 12) are applied to the [A/V OUT] jack directly.
On AM, FM, WFM mode, AF signals from demodulator circuit (RF unit; IC2, pin 9) are applied to the RF amplifier (FM-TV unit; Q71) via J5, pin 1 on RF unit. The amplified signals are applied to the [A/V OUT] jack via the J7, pin 3.

1-7 TFT LCD CIRCUIT (LOGIC UNIT)

The amplified video signal from Q855 on LOGIC unit is amplified at the buffer amplifier (Q903, Q904), and is then applied to the OSD (On Screen Display) IC (IC902, pin 10). The OSD IC produces LCD screen display data, and then outputs video signals to the TFT driver (IC901).
The TFT driver contains the procesing of RGB signal circuit, the color control circuit, etc. The TFT driver controls the TFT LCD (DS4) using the video signals from the OSC IC.

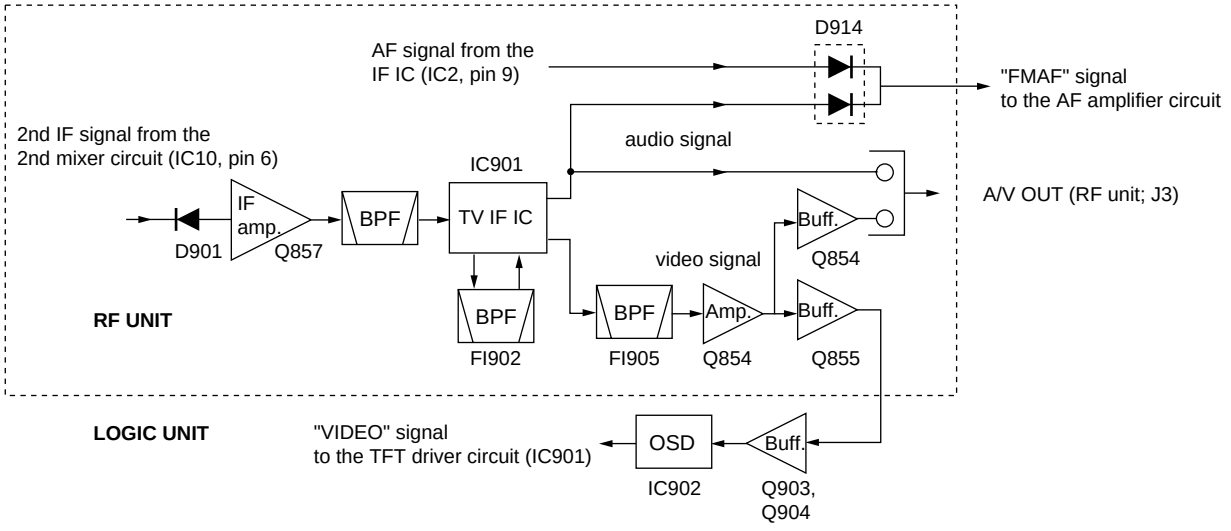
1-8 SQUELCH CIRCUIT (LOGIC AND RF UNITS)

• NOISE SQUELCH

The noise squelch circuit cuts out AF signals when no RF signals are received. By detecting noise components in the AF signals, the squelch circuit switches the AF mute switch.

A portion of the AF signals from the FM IF IC (RF unit; IC2, pin 9) are applied to the active filter section (IC2, pin 8). The active filter section amplifies and filters noise components.

・TV DEMODULATOR CIRCUIT



The filtered signals are applied to the noise detector section and output from IC2 (pin 13) as the “SDET” signal.

The “SDET” signal from IC2 (pin 13) is applied to the CPU (LOGIC unit; IC11, pin 12) directly. The CPU analyzes the noise condition and outputs the “AMUTE” signal to the AF mute switch (Q37).

Even when the squelch is closed, the AF mute switch (Q37) opens at the moment of emitting beep tones.

• TONE SQUELCH

The tone squelch circuit detects AF signals and opens the squelch only when receiving a signal containing a matching subaudible tone (CTCSS). When tone squelch is in use, and a signal with a mismatched or no subaudible tone is received, the tone squelch circuit mutes the AF signals even when noise squelch is open.

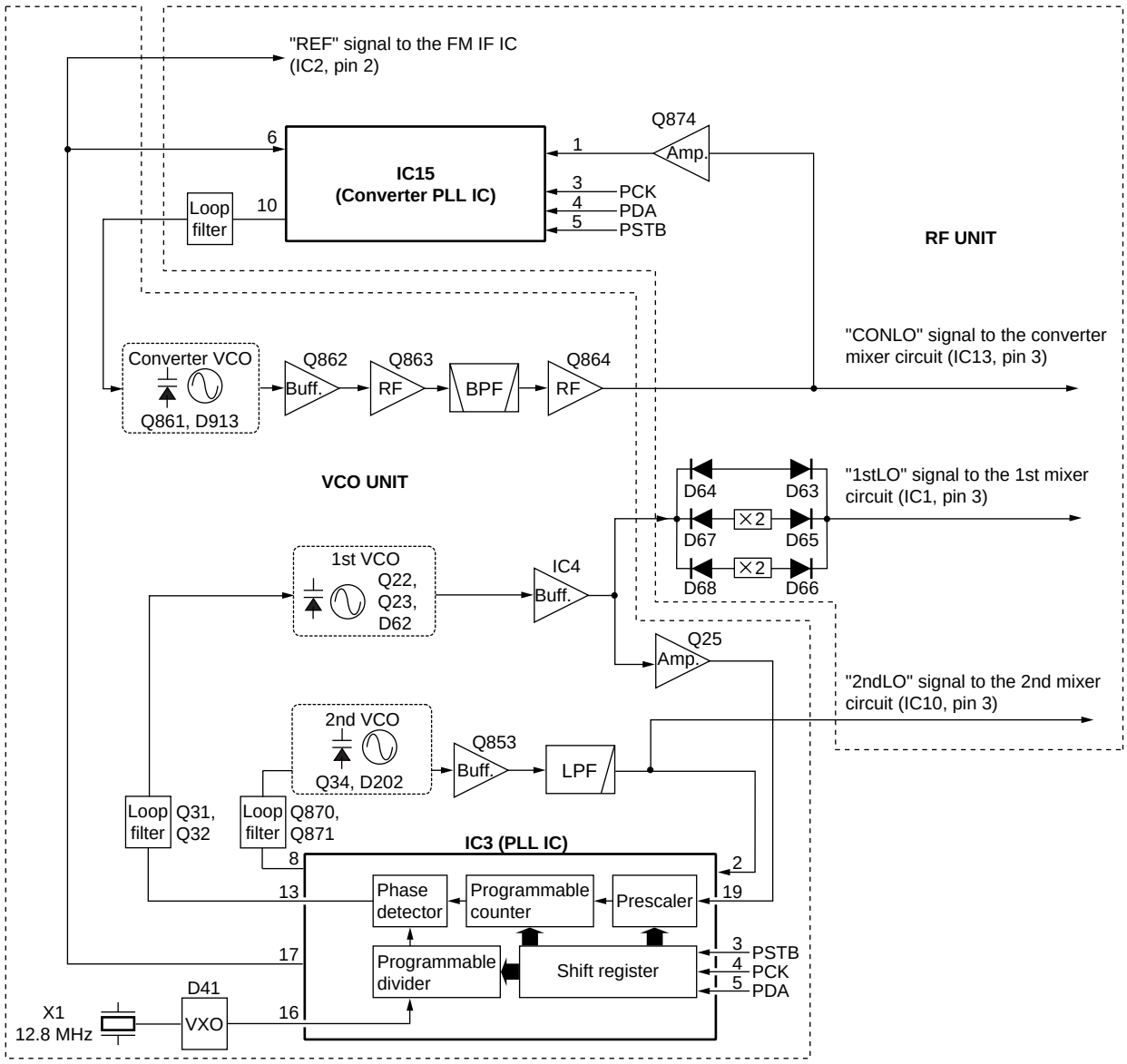
A portion of the AF signals from the FM IF IC (RF unit; IC2, pin 9) passes through the low-pass filter (LOGIC unit; IC9) via the “FMAF” signal to remove AF (voice) signals and passes through the tone filter (LOGIC unit; IC9, Q8). The filtered signal is applied to the CTCSS decoder inside the CPU (LOGIC unit; IC11, pin 8) via the “RTONE” line to control the AF mute switch.

2 PLL CIRCUITS

2-1 PLL CIRCUIT (VCO UNIT)

A PLL circuit provides stable oscillation of the receive 1st/2nd LO frequencies. The PLL circuit compares the phase of the divided VCO frequency to the reference frequency. The PLL output frequency is controlled by the divided ratio (N-data) of a programmable divider.

・PLL CIRCUIT



An oscillated signal from the 1st VCO passes thorough the buffer amplifiers (IC4, Q25) is applied to the PLL IC (IC3, pin 19) and is prescaled in the PLL IC based on the divided ratio (N-data). The PLL IC detects the out-of-step phase using the reference frequency and outputs it from pin 13. The output signal is passed through the loop filter (Q31, Q32) and is then applied to the 1ST VCO circuit as the lock voltage.

2-2 CONVERTER PLL CIRCUIT (RF AND VCO UNITS)

An oscillated signal from the converter VCO is applied to the buffer and amplifiers. The amplified signal passes through the bandpass filter (VCO unit; C972–C979, C981, C982, L921–L924), and is then amplified at the RF amplifier (VCO unit; Q864) and the LO amplifier (RF unit; Q874). The amplified signal is applied to the converter PLL IC (RF unit; IC15, pin 1) and is prescaled in the converter PLL IC based on the divided ratio (N-data). The converter PLL IC detects the out-of-step phase using the reference frequency and outputs it from pin 10. The output signal is passed through the loop filter (RF unit; C956–C958, R945, R946) and is then applied to the converter VCO circuit as the lock voltage.

2-3 REFERENCE OSCILLATOR CIRCUIT (VCO UNIT)

The reference oscillator circuit (X1, IC3) generates a 12.8 MHz reference frequency which is stabilized within the temperature range –10˚C (+14˚F) to +60˚C (+140˚F). The reference frequency is applied to the PLL IC (IC3, pin 16) and the signal is output from the pin 17, and is then applied to the converter PLL IC (RF unit; IC15, pin 6) and the FM IF IC (RF unit; IC2, pin 2).

2-4 1ST VCO CIRCUIT (VCO UNIT)

The oscillated signal is applied to the buffer amplifiers (IC4). The amplified signal is applied to the 1st mixer circuit (RF unit; IC1, pin 3) via the RX LO swtich circuit (RF unit; D63–D68) and the doubler circuit (RF unit; Q25).

The 1st VCO circuit (Q22, Q23, D62) oscillates 240.6 MHz–359.9475 MHz (Low) and 348.1 MHz–520.0475 MHz (High) by switching the SHIFT switch (Q21, D61) “High” and “Low” respectively.

A portion of the signal from IC4 is amplified at the buffer amplifier (Q25) and is then fed back to the PLL IC (IC3, pin 19) as the comparison signal.

2-5 2ND VCO CIRCUIT (VCO UNIT)

The 2nd LO circuit generates the 2nd LO frequencies, and the signals are applied to the 2nd mixer circuit.

The 2nd VCO circuit (Q34, D202) oscillates 183.1–297.1 MHz. The oscillated signal is applied to the 2nd mixer (RF unit; IC10, pin 3), and is then mixed with the 1st IF signal.

An oscillated signal from the 2nd VCO is applied to the buffer amplifier (Q853). The amplified signal passes through the low-pass filter (C154, C250–C252, L69), and is applied to the PLL IC (IC3, pin 2), and is then output from pin 8.

2-6 CONVERTER VCO CIRCUIT (VCO UNIT)

The converter LO circuit generates the converter LO frequencies, and the signals are applied to the converter mixer circuit.

The converter VCO circuit (Q816, D913) oscillates 645.5–675.5 MHz. The oscillated signal is applied to the buffer amplifier (Q862), and is then amplified at the RF amplifier (Q863) to double of oscillate frequency. The 1291–1351 MHz amplified signal is applied to the RF amplifier (Q864) via the bandpass filter (C972–C979, C981, C982, L921–L924). The amplified signal is applied to the converter mixer (RF unit; IC13, pin 3), and is then mixed with the above 1150 MHz RF signal.

An oscillated signal from the converter VCO is applied to the LO amplifier (RF unit; Q874). The amplified signal is applied to the converter PLL IC (RF unit; IC15, pin 1).

3 FM-TV CIRCUIT

3-1 FM-TV CIRCUIT (FM-TV UNIT) ([OTH-2] only includes this unit)

The 426.05 MHz 1st IF signal from the 1st mixer (RF unit; IC1, pin 6) passes through the IF switching diode (D1) via the J6 on the RF unit. The signal is passed through the bandpass filter (FI1) to supress unwanted signal, and then applied tothe IF amplifier (IC1, pin 4). The amplified signal is applied to the FM-TV detector IC (IC2, pin 24 and 25). The FM-TV detector IC contains the AGC amplifier, the loop amplifier, the video amplifier, etc. The video and audio signals are output from the FM-TV detector separately.

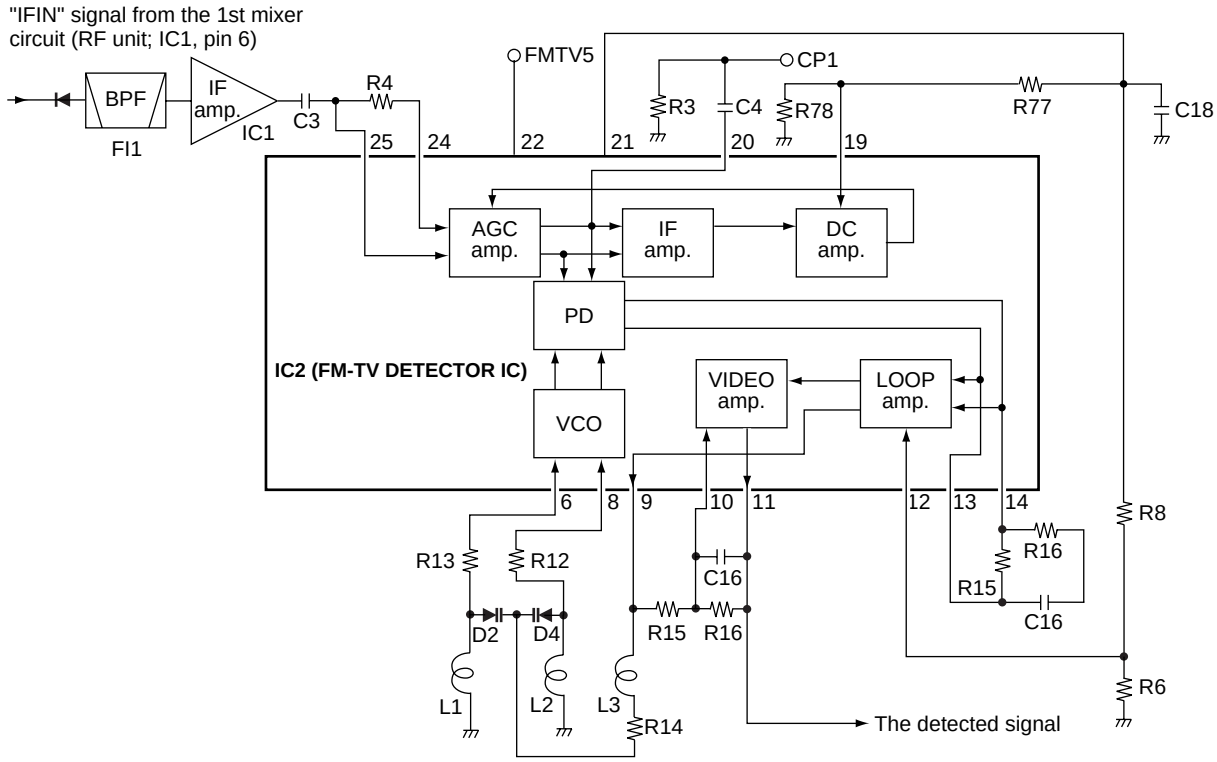
• VIDEO SIGNAL

The detected video signal from the FM-TV IC (IC1) is amplified at the buffer amplifier (Q21), and then applied to the amplifier (IC21, pin 1 and 8). The amplified signal is applied to the video selector IC (IC22, pin 1 and 3) to obtain 6 dB amplification. The amplified signal is output from the video selector IC (pin 7), and is then applied to the buffer amplifier (RF unit; Q855) via the “VIDEO” signal. The amplified signal is applied to the TFT LCD circuit on the LOGIC unit.

• AUDIO SIGNAL

The oscillator (Q51, C53–C55, C57, D51, D52) oscillates 14–28 MHz.
The detected audio signal from the FM-TV IC (IC1) is amplified at the buffer amplifier, and is then applied to the mixer (Q41). The signal is mixed with oscillated 14–28 MHz signal to produce the 13.25 MHz IF signal at the mixer. The IF signal passes through the band switching diode (RF unit; D72) and bandpass filter (RF unit; FI4). The filtered signal is amplified at the 2nd IF amplifier (RF unit; Q41), and is applied to the FM IF IC (RF unit; IC2, pin 16).
The detected signal is applied to the AF circuit (LOGIC unit) for speaker, and applied to the A/V OUT jack (RF unit; J3) via the RF amplifier (Q71).

• FM-TV DETECTOR CIRCUITS (FM-TV UNIT)



4 POWER SUPPLY CIRCUITS

VOLTAGE LINE

LINE	DESCRIPTION
BATV	The voltage from the attached battery.
VCC HV	The same voltage as the BATV line (battery voltage).
+3V	Common 3V converted by the +3V converter circuit (LOGIC unit; Q6, Q39) using the “POWERC” signal from the CPU (LOGIC unit; IC11, pin 28).
3V	Common 3V converted from the VCC line by the +3V regulator circuit (LOGIC unit; IC3). The output voltage is applied to the RESET circuit (LOGIC unit; IC5, pin 2).
R3V	Receive 3V controlled by the R3V regulator circuit (LOGIC unit; Q4, Q5) using the +3SC signal from the CPU (LOGIC unit; IC11, pin 27).
4.5V	Common 4.5V converted from the VCC line by the DC-DC converter (LOGIC unit; IC801). The output voltage is applied to the TFT driver (LOGIC unit; IC901) and the TFT back light driver (LOGIC unit; Q821).
5V	Common 5V converted from the VCC line by the DC-DC converter (LOGIC unit; T1). The output voltage is applied to the OSD IC (LOGIC unit; IC902), etc.
12V	Common 12V converted from VCC line by the DC-DC converter (LOGIC unit; T1). The output signal is applied to the TFT driver (LOGIC unit; IC901).
15V	Common 15V converted from the VCC line by the DC-DC converter (LOGIC unit; T1). The output signal is applied to the TFT LCD (LOGIC unit; DS54).

5 PORT ALLOCATIONS

5-1 EXPANDER IC (RF UNIT; IC5)

Pin number	Port name	Description
5	B1C	Outputs low-pass filter select signal. Low : When frequencies 0.5 to 1.9 MHz are displayed.
6	B2C	Outputs bandpass filter select signal. Low : When frequencies 1.9 to 15 MHz are displayed.
7	B3C	Outputs bandpass filter select signal. Low : When frequencies 15 to 30 MHz are displayed.
8	65MC	Outputs bandpass filter select signal. Low : When frequencies 65 to 108 MHz are displayed.
9	30MC	Outputs bandpass filter select signal. Low : When frequencies 30 to 65 MHz are displayed.
10	SHIFT	Outputs control signal for the VCO shift circuit (VCO unit; Q21, D61). High : While the 1st VCO is shifting.
11	DBL1	Outputs control signal for the doubler1 circuit (RF unit; Q26, D65, D67).
12	DBL2	Outputs control signal for the doubler2 circuit (RF unit; Q26, D66, D68).
16	470MC	Outputs low-pass and bandpass filters select signal. Low : When frequencies 470 to 600 MHz are displayed.
17	600MC	Outputs low-pass and bandpass filters select signal. Low : When frequencies 600 to 750 MHz are displayed.

5-2 CPU (LOGIC UNIT; IC11)

Pin number	Port name	Description
2	THERMC	Input port for the receiver's internal temperature detection.
9	TRACC	Outputs tracking control signal.
10	FSET	Outputs control signal for the RIT frequency.
11	TCON	Outputs control signal for the CTCSS regulator circuit (LOGIC unit; IC9, pin 3). Low : While the CTCSS is ON.
15	VRC	Outputs level control signal for the AF volume.
17	CHGC	Outputs battery charger control signal. High : While battery is charging.
18	AMUTE	Outputs the AF mute switch (LOGIC unit; Q37) control signal. High : While squelched.
19	CLOUT	Outputs the cloning signal.
20	CLIN	Input port for the cloning signal.
21	BEEP	Outputs beep audio signals.
23	POWERC	Outputs the +3V regurator control signals. Low : Power switch is pushed.
24	AFON	Outputs control signal for the AF amplifier regurator circuit. High : Activates the AF amplifier circuit.
25	RXC	Outputs control signal for the receiver regulator circuit.
26	DCDC_C	Outputs the DC-DC converter (LOGIC unit; IC801, pin 2) control signal. Low : While the color LCD is displayed.
27	+3SC	Outputs the +3S regurator control signal.
29	CONVC	Outputs the converter control signal Low : When frequencies above 1150 MHz are displayed.
30	TVC	Outputs control signal for the TV mode. Low : While TV band receiving.
31	LIGHT	Outputs key and LCD backlight control signals. High : Lights ON.
32	CPUHV	Input port for connecting the external power supply detection. Low : While connecting the external power supply.
33	RESET	Input port for the RESET signal.
41	ECK	I/O port for the EEPROM (LOGIC unit; IC2, pin 1) serial clock.
42	ECS	Outputs chip select signal for the EEPROM (LOGIC unit; IC2, pin 1).
45	PSTB	I/O port for strobe signal from/to the PLL IC (VCO unit; IC3, pin 3).
51	OSSTB	Outputs chip select signal for the color LCD.
52	TGSTB	Outputs the color LCD load signal
54	DATA	Outputs the color LCD control signal. Outputs serial data for the LCD controllor.
56	UHF3VC	Outputs bandpass filter select signal. Low : When frequencies 330 to 470 MHz are displayed.
57	174MC	Outputs bandpass filter select signal. Low : When frequencies 174 to 225 MHz are displayed.
58	108MC	Outputs bandpass filter select signal. Low : When frequencies 108 to 174 MHz are displayed.
59	HFC	Outputs control signal for the HF band receiver regurator circuit (RF unit; Q5). Low : When frequencies 0.5 to 30 MHz are displayed.
60 61 62	ATT3 ATT2 ATT1	Outputs attenuater control signal. High : While attenuater is ON.
63	AM	Outputs AM mode select signals. Low : When AM is selected.
64	WFM	Outputs WFM mode select signals. Low : When WFM is selected.